



TRANSMITTAL FORM

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Total Number of Pages in This Submission

Application Number

10/736,908

Filing Date

12/17/2003

First Named Inventor

Frederic Joso et al.

Art Unit

2123

Examiner Name

TBD

Attorney Docket Number

003921.00137

ENCLOSURES (check all that apply)

- Fee Transmittal Form
 - Fee Attached
- Amendment / Reply
 - After Final
 - Affidavits/declaration(s)
- Extension of Time Request
- Express Abandonment Request
- Information Disclosure Statement
- Certified Copy of Priority Document(s)
- Response to Missing Parts/ Incomplete Application
- Response to Missing Parts under 37 CFR 1.52 or 1.53

- Drawing(s)
- Licensing-related Papers
- Petition
- Petition to Convert to a Provisional Application
- Power of Attorney, Revocation Change of Correspondence Address
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- After Allowance Communication to Group
- Appeal Communication to Board of Appeals and Interferences
- Appeal Communication to Group (Appeal Notice, Brief, Reply Brief)
- Proprietary Information
- Status Letter
- Other Enclosure(s) (please identify below):
Forms - PTO/SB/08a & PTO/SB/08b, one copy of two foreign documents and nine non-U.S. patent documents

Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm
or
Individual name

John M. Fleming, Reg. No. 56,536

Signature

Date

March 8, 2005

CERTIFICATE OF TRANSMISSION/MAILING

I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below.

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This collection of information is required by 37 CFR 1.5. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.



PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:

Frederic Josso et al. : Confirmation No.: 4026
Application No. 10/736,908 : Group Art Unit: 2123
Filed: December 17, 2003 : Examiner: TBD
For: Distributed Configuration of : Atty Docket: 003921.00137
Integrated Circuits In An
Emulation System

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Sir:

Pursuant to the duty of disclosure under 37 CFR §§ 1.56 and 1.97-1.98, the documents listed on the attached forms, PTO/SB/08a and PTO/SB/08b, are being brought to the attention of the Examiner in charge of the above-identified application. Copies of the cited U.S. patents and are not enclosed. Copies of the foreign patent documents and non-patent literature documents are enclosed, in accordance with 37 C.F.R. § 1.98(a)(2).

The Examiner is respectfully requested to initial the spaces adjacent the documents entry on the PTO forms, and to return a copy of the initialed PTO Forms to confirm that the documents have been considered and has been officially made of record in this application.

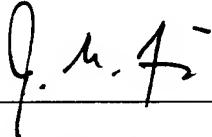
If the Examiner has any questions or wishes to discuss this application, the Examiner is invited to telephone the undersigned representative at the number set forth below.

The accompanying Supplemental Information Disclosure Statement is being filed before the mailing date of a first Office Action on the merits. Therefore, no fee is believed due at this time. In the event there is a discrepancy with the fee, please charge or credit Deposit Account No. 19-0733. Further, the Commissioner is authorized to charge any additional fees that may be required or credit any overpayment to our Deposit Account No. 19-0733.

Respectfully submitted,

BANNER & WITCOFF, LTD.

Date: March 8, 2005

By: 

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11th Floor
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John M. Fleming
Registration No. 56,536



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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 2

Street | City | State | Zip | E-mail | Attorney Docket Number | 000021.00137

U.S. PATENT DOCUMENTS

Examiner Initials *	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code ² (if known)			
		US- 4,860,290	08-22-1989	Daniels et al.	
		US- 5,036,473	07-30-1991	Butts et al.	
		US- 5,109,353	04-28-1992	Sample et al.	
		US- 5,572,710	11-05-1996	Asano et al.	
		US- 5,596,742	01-21-1997	Agarwal et al.	
		US- 5,777,489	07-07-1998	Barbier et al.	
		US- 5,821,773	10-13-1998	Norman et al.	
		US- 5,870,586	02-09-1999	Baxter	
		US- 5,943,490	08-24-1999	Sample	
		US- 6,002,861	12-14-1999	Butts et al.	
		US- 6,184,707	02-06-2001	Norman et al.	
		US- 6,265,894 B1	07-24-2001	Reblewski et al.	
		US- 6,282,503	08-28-2001	Okazaki et al.	
		US- 6,377,912 B1	04-23-2002	Sample et al.	
		US- 6,388,465	05-14-2002	Barbier et al.	
		US- 6,473,726 B1	10-29-2002	Reblewski	
		US- 6,625,793 B2	09-23-2003	Sample et al.	
		US- 6,694,464 B1	02-17-2004	Quayle	
		US- Re. 34,363	08-31-1993	Freeman,deceased	

FOREIGN PATENT DOCUMENTS

Examiner Signature		Date Considered	
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¹EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ² Applicant's unique citation designation number (optional). ³ See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ⁴ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁵ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁶ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁷ Applicant is to place a check mark here if English language Translation is attached.

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Substitute for Form 1449B/PTO

INFORMATION DISCLOSURE
STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet

2

of

2

Complete if Known

Application Number	10/736,908
Filing Date	12/17/2003
First Named Inventor	Frederic Joso et al.
Art Unit	2123
Examiner Name	TBD

Attorney Docket Number 003921.00137

NON PATENT LITERATURE DOCUMENTS

Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		Erhard et al., W. First Steps Towards a Reconfigurable Asynchronous System, IEEE International Workshop on Rapid System Prototyping, 1999, pgs. 28-31	
		Kocan et al., F. Concurrent D-Algorithm on Reconfigurable Hardware, IEEE/ACM International Conference on Computer-Aided Design, 1999, Digest of Technical Papers, pgs. 152-155	
		Clos, Charles, "A study of Non-Blocking Switching Networks," The Bell System Technical Journal, March 1953, pgs. 406-424	
		Bosi et al., B. Reconfigurable Pipelined 2-D Convolvers for Fast Digital Signal Processing, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 7, Issue 3, Sept. 1999, pgs. 299-308	
		Ejnioui et al., A. Design Partitioning on Single-Chip Emulation Systems, 13 th International Conference on VLSI Design, 2000, pgs. 234-239	
		Jean, J.S.N., et al., "Dynamic Reconfiguration to Support Concurrent Applications," IEEE Transactions on Computers, June 1999, IEEE, USA, vol. 48, No. 6, pgs. 591-602	
		Snider, G., "The Teramac Compiler," Nov. 29, 1993, pgs. 1-51	
		Xilinx, "The Programmable Gate Array Design Handbook", First Edition, 1986, pgs. i-A10	
		Babb, J. et al., "Logic Emulation with Virtual Wires," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, June 1997, pgs. 1-20	

Examiner Signature	Date Considered
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹Applicant's unique citation designation number (optional). ²Applicant is to place a check mark here if English language Translation is attached.

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